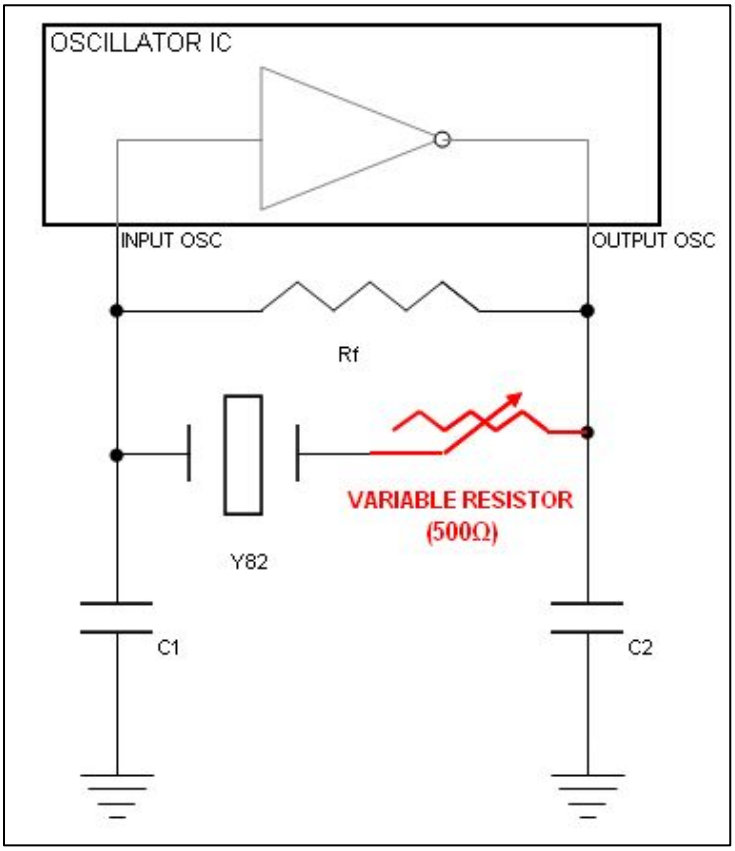
Technical Information & Training Document

NEGATIVE RESISTANCE CHECK 负性阻抗检查

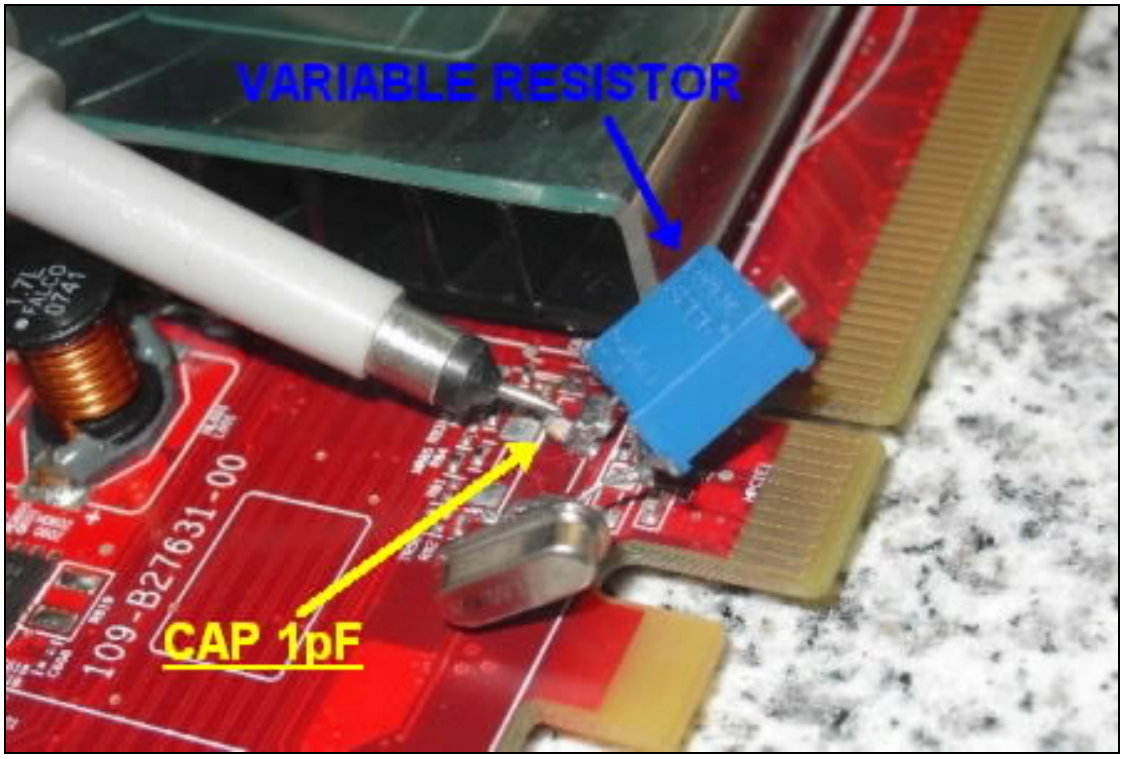
In order to determine the Circuit Margin (CM) the negative resistance shall be determined first. 为了确定电路 Margin(CM)，需要首先确定负性阻抗。
In order to determine the negative resistance, we have to check the maximum crystal resistance that the oscillator circuit could drive. 为了确定负性阻抗，我们必须检查振荡电路可以激励的晶体最大电阻。



To measure negative resistance, we add a variable resistor (pot) in series with the quartz crystal unit. When selecting the pot, we suggest starting with a 500Ω pot. For high gain circuits or low frequency circuits, a 1kΩ pot may be needed. Once the pot is assembled on PCB and board power up, the resistance is slowly increased until oscillation stops. Resistance is then decreased until oscillator circuit just starts working. The variable resistor (pot) is then removed and resistance measured on an ohmmeter. 为了测量负性阻抗，我们与晶体串联一个可调电阻（变阻器）。选择变阻器时，我们建议先选一个 500 欧的变阻器。对以高增益电路或低频率电路，需要一个 1kΩ 变阻器。一旦把变阻器装在板上并通电，渐渐增大电阻直到振荡停止。然后减小电阻直到振荡电路开始工作。然后拆下这个可调电阻（变阻器），并在欧姆计上测量电阻。

The crystal used MUST be an average crystal. Do NOT test a defective, questionable, or unknown crystal for this negative resistance test. 使用必须是一个一般的晶体。不要在测试负性阻抗时使用一个不良的，有问题的或未知的晶体。

For testing purposes, the board was plugged into a PC motherboard in order to provide proper power supply. Test circuit consisted of an Agilent 500MHz oscilloscope used with probe as well as HP 225 MHz frequency counter and an multimeter. 为了测试，把板子装在一个电脑主机上以提供足够的电源。测试电路包括一个有探针的安捷伦 500MHz 示波器，以及 HP225MHz 频率计和一个万用表。



The results of these measurements are 这些测量的结果是:

Board #1 the resistance value was determined with 板#1 的电阻确定为 R_{TEST} = 44.6Ω
Board #2 the resistance value was determined with 板#2 的电阻确定为 R_{TEST} = 37.6Ω

Once we have dynamically tested the circuit's ability to start an average crystal, we can calculate the Negative Resistance (–r) using the below equation shown in figure 2. 一旦我们动态地测试了电路起振一个一般晶体的能力后，我们可以用以下图 2 中的公式算出负性阻抗（-r）.

Figure 2

$$-r = R_{TEST} + ESR$$

That requires also the Effective Series Resistance (ESR) of the crystal which is defined as shown in below. 这还需要知道晶体 ESR(等效串联电阻)，见以下公式。

Figure 3

$$ESR = R_1\left(1+\frac{C_0}{C_L}\right)^2$$

A premeasured, average crystal with following parameters was used. You may ask your crystal manufacturer for assistance in providing these data. R1 in equation above is equal to the RR or Rs shown as crystal resistance in data printout of your crystal manufacturer. 使用一个之前测试过的，有以下参数的一般晶体。你们可以问你们的晶体产商协助提供这些数据，上面公式中的 R1 等于你们晶体厂商打印数据中用来表示晶体电阻的 RR 或 Rs。

Resistance	RR	9.3Ω
Shunt capacitance	C0	3.0pF
Load capacitance	CL	18.0pfF

Using above data of our test crystal we can calculate ESR as 使用我们测试晶体的上述数据，我们可以算出 ESR 为:

Figure 3a) $$ESR = 9.3\Omega\left(1+\frac{3.0\,pF}{18.0\,pF}\right)^2$$

Figure 3b) $$ESR = 12.7\Omega$$

Having ESR calculated we can now determine the negative resistance for both boards based on equation shown in figure 2. The negative resistance is the sum of the measured resistance R_{TEST} and the ESR of the tested crystal unit. 算出 ESR，根据图 2 中的公式，现在我们可以确定这两块板的负性阻抗。负性阻抗为量测出的电阻与测试的晶体 ESR 之和。

Board #1 R_{TEST} = 44.6Ω gives us **negative resistance of 57.3Ω**
Board #2 R_{TEST} = 37.6Ω gives us **negative resistance of 50.3Ω**

OSCILLATOR CIRCUIT MARGIN DETERMINATION 确定振荡电阻 Margin

With the negative resistance measurement, we can calculate the Circuit Margin for the given oscillator on the board. The Circuit Margin is defined as the absolute value of negative resistance $|-r|$ divided by the average value of Effective Series Resistance (ESR). Formula for circuit margin is as shown in figure 4. 测出了负性阻抗，我们可以算出板上给该振荡器的电路 Margin。这个电路 Margin 的定义为负性阻抗的绝对值$|-r|$除以 ESR 的平均值。图 4 是电路 Margin 的公式。

Figure 4 $$CM = \frac{|-r|}{ESR_{AVG}}$$

The ESR AVERAGE that should be used here is referring to the average ESR of a certain crystal batch since the crystal units resistance is spreading over a certain range due to manufacturing tolerances. 这里应该使用的 ESR 平均值是指一定晶体批次的平均 ESR，因为生产的容许偏差，这些晶体的电阻会分布于一定范围内。

Taking equation in figure 4 and ESR value of our test crystal unit (ESR = 12.7Ω) we are getting the following circuit margin for the two examined boards 使用图 4 中的公式是我们测试晶体的 ESR 值（ESR=12.7 Ω），我们将得到这两块测试的板的电路 Margin:

Board #1 $|-r|$ = 57.3Ω gives us a low **circuit margin CM of only 4.5**
Board #2 $|-r|$ = 50.3Ω gives us a low **circuit margin CM of only 4.0**

Q: What should the Circuit Margin be? 电路 Margin 应该是多少呢？
A: Should be over 10. Must be absolute minimum of 5.0. 应该大于 10。必须至少 5.0。

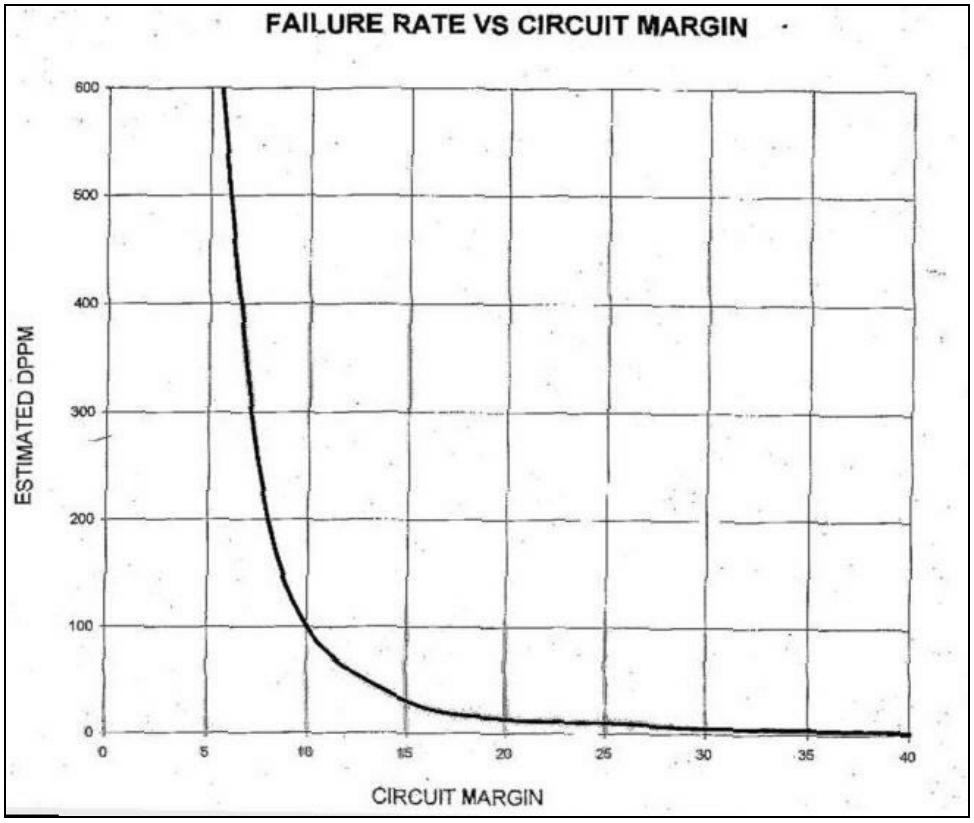
OSCILLATOR CIRCUIT MARGIN RELATIONSHIP TO EXPERIENCED FAILURE RATE 振荡电路 MARGIN 与预计不良率之间的关系

Poor Circuit Margin correlates directly into the failure rate during board manufacturing and customer use. 差劲的电路 Margin 直接与电路板生产和客户使用中的不良率有关。

Below chart show the relationship between circuit margin and expected failure rate in board manufacturing. The abscissa is Circuit Margin. The ordinate is defect rate – dppm. Please observe – using the same crystal 以下图表表示了电路 margin 与电路板生产中预计的不良率之间的关系。横坐标是电路 margin。纵坐标是不良率-dppm。请看----使用相同晶体:

- A CM of 4.5 is off the graph – probably several thousands of dppm. CM4.5 不在曲线内----很可能几千 dppm.
- A CM of 5 is also off the graph – probably about 1k dppm. CM5 也不在曲线内----很可能 1 千 dppm.
- A CM of 6 is ~800 dppm
- A CM of 10 is ~100 dppm

- A CM of 15 is ~35 dppm



When necessary to vary the PCB's Circuit Margin, we need to consider the PCB factors generating the negative resistance. If we look at the negative resistance, we can say 如果需要改变 PCB 的电路 Margin, 我们需要考虑产生负性阻抗的 PCB 的一些因素。如果我们看看负性阻抗，我们可以说:

Figure 6

$$-r = gm \times \left(\frac{1}{\omega C_1} \times \frac{1}{\omega C_2} \right)$$

Where gm is the transconductance of the circuit. 这里 gm 是电路的互导（跨导）。

This formula shows us our load capacitors C_1 and C_2 both in the denominator, which means that the negative resistance will increase if we reduce the values of either or both of the two pi capacitors. We could say that the capacitor values give us some "handles" to work with. 这个公式告诉我们我们的负载 C1 和 C2 都在分母上，这意味着如果我们降低任意一个或两个 pi 电容，负性阻抗就会增大。我们可以说电容值给了我们一些可以考虑的解决方法。

The voltage gain from back to front of circuit should be another consideration. Usually C1 and C2 are equal, or C1 is slightly smaller than C2. If we consider the signal on both sides of the crystal, which is the same as both ends of the amplifier, we can say the voltage gain from back to front is equal to C_2/C_1. Often C2 is slightly larger to make up for losses through the crystal and to have a lower value impedance loading the IC OUTPUT.. 电路前后的电压增益应该是另一个考虑因素。通常 C1 和 C2 是相等的，或 C1 稍微小于 C1。如果我们考虑晶体两侧的信号，这与放大器两端是一样的，我们可以说前后的电压增益等于 C_2/C_1。通常 C2 会稍微大一点，以弥补通过晶体时的损耗，以及在 IC 输出端获得一个较小的阻抗。

SUGGESTION TO SOLVE THE PROBLEM 解决这个问题的建议

In order to improve Circuit Margin performance, it is suggested to lower the load capacitance of the circuit. This would comply better to the frequency that the oscillator running at and it would also increase the circuit margin to some extend. 为了改善电路 margin，建议降低电路的负载。这将会改善振荡器的频率，并将一定程度的增大电路 margin。

However if C1 and C2 are reduced in value, this will also cause higher impact of board variation, component tolerances and crystal unit variations due to the increase of crystals pullability. It will also increase the cost due to the fact that the higher pullability will also cause higher cost in manufacturing if not even becoming non-producible. Therefore it is depending on the customer to make this decision based on the board's total frequency tolerance. 但是如果减小 C1 和 C2 的值，由于晶体牵引的增大，这样做的话也会导致受电路板差异，元器件容许偏差以及晶体差异的影响更大。

In case customer decides to change the load capacitance of the circuit we suggest the following 如果客户觉得改变电路板的负载，我们有以下建议:
In order to get a 14pF total load we have to consider the large stray capacitance of over 7pF and deduct it from the 14pF we need at the end. Therefore we are looking for values of C1 and C2 that will calculate out to a total capacitance of 6 to 7pF. 为了获得总负载 14pF，我们必须考虑超过 7pF 的离散电容，用最后我们需要的 14pF 减去它。这样我们知道 C1 和 C2 通过计算总电容是 6 到 7 pF。

We also suggest using two unequal values by making C2 slightly larger in order to get better voltage gain and make up for losses. For this purpose it is suggested to make C2 about 20~30% larger than C1. 我们也建议使用两个不等的值，使 C2 稍微到一点，这样可以获得更佳的电压增益并弥补损耗。为此，建议使 C2 比 C1 到 20~30%。

As shown above, the oscillator cell is not providing enough circuit margin in order to guaranty proper startup of the circuit under all conditions. Up to this point other conditions such as behavior at different temperatures had not been evaluated and may worsen the findings above. 正如上面所说，振荡器单元没有提供足够的电路 margin 正如上面所说，振荡器单元没有提供足够的电路 margin 来保证电路在所有条件下都能很好的起振。到此，其他条件，比如不同问题时的表现都尚未进行评估，并会使以上的发现更为糟糕。
Therefore we would like to make sure that it is being understood that ONLY a design change of the oscillator cell would be a good solution, all other ways may reduce the failure rates but cannot be seen as the correct solution. 所以我们希望确保你们能够知道，只有振荡单元设计的变更才会是好的解决方法，其他方式肯降低不良率但是不会是正确的解决方案。
We are not the oscillator designer and declare that above made suggestions are by best of our knowledge but we do not guaranty satisfaction nor any do we consider us a liable for any damages that may occur when above stated changes being implemented. 我们不是振荡器的设计者，并声明以上的建议就我们所知，但是不保证满意度，并且我们不认为我们对一旦上述变更实施后的任何损害负有责任。

Respectfully

M. Bruech		*June 7th 2009*
QA Mgr. of NKG/RT		Date: